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SILICON BIPOLAR DISTRIBUTED OSCILLATOR DESIGN AND ANALYSIS

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ABSTRACT
The design of high frequency silicon bipolar oscillator using common emitter (CE) with distributed output and analysis is carried out. The general condition for oscillation and the resulting analytical expressions for the frequency of oscillators were reviewed. Transmission line design was carried out using Butterworth LC filters in which the normalised values $\mathbf{L_n}$ and $\mathbf{C_n}$ where used to obtain the actual values of the inductors and capacitors used; this largely determines the performance of distributed oscillators. The values of inductor and capacitors in the phase shift network are used in tuning the oscillator. The simulated results show that the oscillator operates at 26MHz, dissipating 15mW power. The result indicates that distributed amplification methodology is viable at high frequency.

Keywords: Silicon, Oscillator, Bipolar, Design, Analysis.

INTRODUCTION
The rapid-increasing demand for large bandwidth in the digital and analogue market, wired or wireless is making it necessary to operate integrated circuit at higher frequencies. In today's electronics world, silicon specifically complementary metal oxide semi conductors (CMOS), has emerged as a promising low-cost alternate for RF and microwave circuits. Moreover, silicon based circuits are highly suitable for system on-chip implementations. However, silicon suffers from large parasitic elements both in active and passive devices, and therefore new design approaches are highly needed at such high frequency (Wu and Hajimiri, 2001).

Dividing design objective has been the underlying principle used to solve many engineering and social problems. Conventional circuit design is a very well defined level of abstraction between device physics and system theory. In conventional electronic design, circuit elements such as transistors, resistors and capacitors are defined by their voltage-current characteristics in time and frequency domain which are nonlinear in general. The accuracy of the analysis can be improved by including the parasitic components caused by second order effects in the device model.

Distributed circuits can defy some of the performance trade-offs in conventional circuits by taking advantage of multiple parallel signal paths. This multiple signal path feature of the distributed systems often results in strong electromagnetic couplings between circuit components across multiple levels of abstraction. The term *distributed* has been used in various contexts with different meanings, however in our treatment, a system will be called distributed if it uses multiple parallel signal paths and devices working in harmony to perform a desired task. The operation of the amplifier can be understood more easily using the transmission-line-based version of the amplifier. The extended bandwidth of the distributed amplifier comes at the price of a larger time delay between its input and output. It can be shown that there is a trade-off between the bandwidth and delay in an amplifier (Lee, 1998). Distributed amplification provides a means to take advantage of this trade-off in applications where the delay is not a critical specification of the system and can be compromised in favour of the bandwidth (distributed oscillator). It is noteworthy that the physical size of a distributed amplifier does not have to be comparable to the wavelength for it to enhance the bandwidth. Dividing the gain between multiple active devices avoids the concentration of the parasitic at one place and hence eliminates a dominant pole scenario in the frequency domain transfer function. Here, one tries to avoid a weakest link situation by providing multiple equally strong (or equally weak) parallel paths for the signal. In the case of a distributed amplifier, each pathway provides some gain; therefore, the whole amplifiers capable of providing a higher gain-bandwidth product than a conventional amplifier. A good understanding of transmission lines is essential to the design of high speed.

Transmission line theory can now be utilized to determine the effective transmission line parameters, characteristic impedance and propagation constant of each line. An electronic oscillator may be defined in any one of the following four ways

i. It is a circuit which converts dc energy into ac at very high frequency;
ii. It is an electronic source of alternating current or voltage having sine, square or saw-tooth or pulse shapes;
iii. It is a circuit which generates an ac output signal without requiring any externally applied input signal;
iv. It is unstable amplifier.

These definitions exclude electromechanical alternators producing 50Hz ac power or other devices which convert mechanical or heat energy in to electric energy.

Comparison can be made between an amplifier and an oscillator. An amplifier produces an output signal whose waveform is similar to the input signal but whose power level is generally high; this additional power is supplied by the eternal dc source. Hence, an amplifier is essentially an energy converter i.e. it takes energy from the dc power source and converts it into ac energy at signal frequency the process of energy conversion is controlled by the input signal. If there is no input signal, there is no energy conversion and hence there is no output signal. An oscillator differs from an amplifier in one basic respect. The oscillator does not require an external signal either to start or maintain energy conversion process. It keeps producing an output signal so long as the dc power is connected. Moreover, the frequency of the output signal is determined by the passive components used in the oscillator and can be varied at will.

Electronic oscillators may be broadly divided into the

following two groups; sinusoidal and non sinusoidal. Ultimately, the amplitude of the oscillations decays to zero when there is not enough energy to supply circuit losses. However, the frequency or time period remains constant it is determined by the circuit parameters (Ayasli, *et al.*, 1982).

OPERATIONAL THEORY OF DISTRIBUTED OSCILLATOR

The operation of the distributed oscillator can perhaps be most easily understood when explained using Figure 1. The distributed oscillator consists of a pair of transmission lines .

with characteristic impedances of Z_O independently connecting the inputs and outputs of several active devices. An RF signal is thus supplied to the section of transmission line connected to the input of the first device. As the input signal propagates down the input line, the individual devices respond to the forward travelling input step by inducing an amplified complementary forward travelling wave on the output line. Terminating resistors Z_b and Z_c are placed to minimize destructive reflections

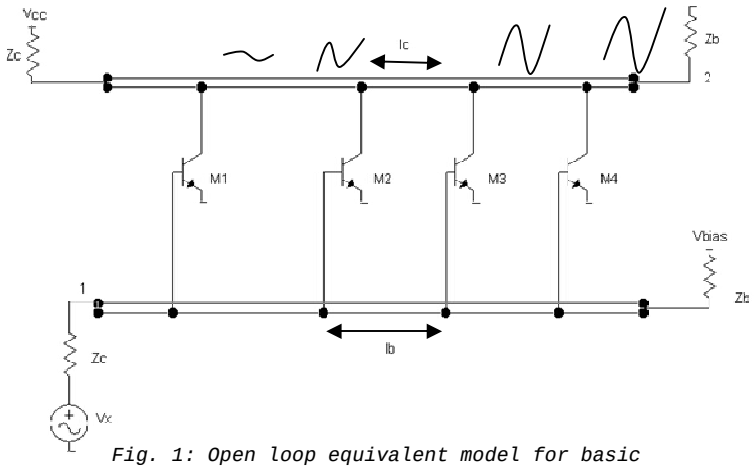

Fig. 1: Open loop equivalent model for basic

Denoting the transconductive gain of each device as g_m and recognizing that the output impedance seen by each transistor is half the characteristic impedance of the transmission line one arrives at the overall voltage gain of the distributed amplifier (DA) being (Hajimiri, A. 2002).

$$A_V = ng_m\frac{Z_0}{2} \qquad (1)$$

where n is number of transistors and Z_0 the characteristic impedance.

Neglecting losses, the gain demonstrates a linear dependence on the number of devices (stages). Another limiting feature of large-sized devices within the context of the distributed amplification is revealed when considering the Bragg cut off frequency of the parasitically loaded transmission lines. The Bragg cut off frequency (ω_C) of the transmission lines within a distributed matching network can be roughly computed using

$$\omega_C = \frac{2}{\sqrt{L_T + (C_T + C_{devices})}} \qquad (2)$$

where *L* is the total inductance of the line segment T and *C* is the sum of the line segment capacitance and the parasitic loading capacitance upon the line segment (Lee, 2004).

For the analysis of distributed oscillators, a distributed oscillator (Figure 1) operates in the forward-gain mode of a distributed amplifier. The forward wave on the base line is amplified by each transistor and appears on the collector line. The travelling wave on the collector line travels to the right in synchronization with the travelling wave on the base line. Each transistor adds power in phase to the signal at each tapping point on the collector line. Thus, the forward path can have an overall gain larger than unity while the gain of each transistor may be less than one. To sustain oscillations, the output of the collector line (node 2) is fed back to the input of the base line (node 1).

The forward travelling wave on base line and the backward (travelling to the left) wave on the collector line are absorbed by terminations matched to loaded characteristic impedance of the base line and collector line respectively. In steady state, the gain from 1 to 2 should be unity. For a large coupling capacitor, the nodes 1 and 2 should have identical ac voltages. In the most general case, the load impedance of the base and collector lines are not equal, so it is important to have the correct source and load impedance at nodes 1 and 2 to consider loading effects. The voltage at the *i*th tap of the base line is related to the base line's segment length, l_b and complex transmission line propagation constant, γ_b through the relation

$$V_{bi} = V_1 e^{-(i-1)\gamma_b i_b} \qquad (3)$$

where V_I is the voltage at node 1. This is assuming that the base line is terminated to the loaded characteristic impedance of the base line, given by

$$Z_b = \sqrt{\frac{j\omega L_b + R_b}{j\omega\left(C_b + \frac{C_\pi}{i_b}\right) + G_b}} \qquad (4)$$

where L_b, R_b, C_b, and G_b are the series inductance, resistance, parallel capacitance and conductance of the base transmission line per unit length, respectively and C_π is

the small signal base-emitter capacitance of the bipolar transistors. Assuming that the collector line is terminated to its loaded characteristic impedance,

$$Z_c = \sqrt{\frac{j\omega L_c + R_c}{j\omega\left(C_c + \frac{C_{out}}{i_c}\right) + G_c}} \quad (5)$$

where L_c, R_c, C_c, and G_c are the series inductance, resistance, parallel capacitance and conductance of the base transmission line per unit length respectively and C_{out} is the total output capacitance of the bipolar transistors. Note that the impedance seen by the incident wave is the characteristic impedance of the transmission line. The generated incident wave at the *i*th collector tap travelling to the right is therefore given by:

$$E_{ci} = -G_m \frac{Z_c}{2} V_{bi} = -G_m \frac{Z_c}{2} V_1 e^{-(i-1)\gamma_b i_b} \quad (6)$$

where G_m is the large signal transconductance of each transistor as defined in (Clarke and Hess, 1971). These generated waves travel through different lengths of transmission line to get to the output node. Therefore, the total incident wave at node **2** is given by superposition, as

$$E_{i2} = \sum_{i=1}^{n} E_{ci} e^{-(n-i+1)\gamma_c i_c} \quad (7)$$

Part of this incident wave will be reflected due to the impedance mismatch at node 2 as the collector line is connected to the base line which generally has different loaded characteristic impedance. The reflected wave, E_{r2}, is related to the incident wave, E_{i2}, through the reflection coefficient, Γ_2

$$\Gamma_2 = \frac{E_{r2}}{E_{i2}} = \frac{Z_b - Z_c}{Z_b + Z_c} \quad (8)$$

The voltage at node 2 will thus be given by

$$V_2 = E_{i2} \frac{2Z_b}{Z_b + Z_c} \quad (9)$$

Using equation 6, 8 and 9, V_2 can be expressed in terms of V_1. Noting that for steady-state oscillations, as they represent the same ac node in closed loop system, the following general oscillation condition is obtained:

$$G_m(Z_b \parallel Z_c) \frac{e^{-(n+1)\gamma_c i_c} - e^{-(n+1)\gamma_b i_b}}{e^{-\gamma_c i_c} - e^{-\gamma_b i_b}} = 1 \quad (10)$$

This condition determines both the amplitude and the frequency of the oscillation respectively given by

$$V_{amp} = \frac{2i_c}{G_m} = 2ni_c(Z_b \parallel Z_c)e^{-\alpha nl} \quad (11)$$

and

$$f_0 = \frac{v_{group}}{2nl} \quad (12)$$

where $e^{-\alpha nl}$ represents the loss in the transmission line and v_{group} is the wave group velocity in the line. It is noteworthy that equation 11 reduces to the expression for the amplitude of a lumped oscillator for *n* =1 (Lee, 1998).

CALCULATION OF COMPONENTS VALUES

The method used was the simulation method using Multisim 8.0 Electronics workbench, a simulation and circuit design software. $BC107\ PNP$ Transistor was chosen from the bipolar transistor family due to the fact that it is a general purpose transistor with high forward current gain and small saturation current. The input-base characteristics were obtained and a graph of $I_B(\mu A)$ and $V_{BE}(v)$ at constant value of $V_{CE}(v)$ plotted and the input-characteristics curve obtained (Fig.2). Using the data obtained for the output characteristics, a graph of $I_C(mA)$ versus $V_{CE}(v)$ was plotted and a family of the characteristic curves drawn (Fig.3). From the output characteristic curves, the bias voltage V_{CE} was determined. The V_{CC} (dc supply) battery was chosen along V_{CE} axis, the V_{CE} equal to halve V_{CC} i.e. $\frac{1}{2}V_{CC}$ (Boylestad *et al.*, 2006). By simply choosing a particular value of base current (I_B), the operating or Q-point was located at the intersection of the selected values. $I_C(mA), V_{CC}(V), V_{CE}(V)\ and\ I_B(\mu A)$ which are the operating points were all obtained from the curve. The remaining amplifier component parameters were calculated using the procedure in (Benedict, 1976).

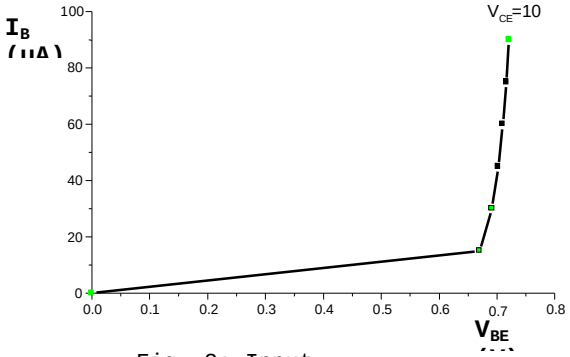

Fig. 2: Input Characteristic

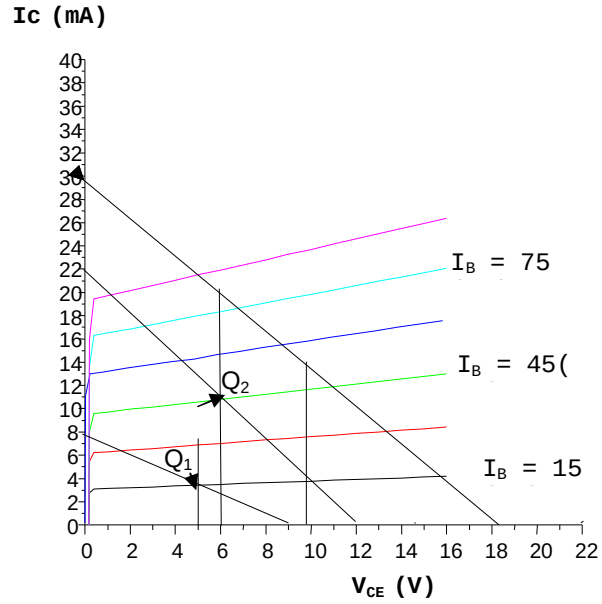

Fig. 3: Output Characteristics for BC 107 Transistor

DESIGN EQUATIONS

The value of R_E chosen ($R_E \approx 0.2R_C$), load line drawn for (R_C + R_E) on the collector characteristics and the Q point excursion on the load line is chosen. Power dissipation is determine using

$$P_d = V_{CE}I_C \quad (13)$$

The value of I_C was determined from the graph. The following equations were used

$$R_B = 0.3\beta R_E \quad (14)$$

$$V_{BB} = I_B R_B + V_{BE} - I_E R_E \quad (15)$$

$$R_1 = \frac{V_{cc}R_B}{V_{cc}-V_{BB}}, \quad R_2 = \frac{V_{cc}R_B}{V_{BB}}, \quad R_C = \frac{V_{CE}}{I_C} \quad (16)$$

C_I *and* C_E were calculated using,

$$C_c = \frac{10}{\omega(h_{ie}+R_s)} \qquad C_E = \frac{h_{fe}}{\omega(h_{ie}+R_s)} \quad (17)$$

$$g_m r_\pi = \beta, \text{ where } = \frac{I_C}{I_B}, \quad (18)$$

Also $g_m = \frac{I_{cq}q}{KT} \approx 40 I_C mA$ (19)

$$r_\pi = h_{ie} \quad (20)$$

THE COMMON EMITTER (CE) AMPLIFIER

The following values were used to produce the single stage common emitter (CE) amplifier (Fig.4) and the corresponding simulated waveform of the CE amplifier (Fig.5).

$V_{CC} = 9V$, $V_{CE} = 4.5V$, $V_{BE} = 0.7V$
$I_C \cong I_E = 3.4mA$, $I_B = 15\mu A$, $V_{BB} \approx 1.8V$,
$P_d \approx 15mW$, $R_E = 265\Omega$, $\beta = 227$
$g_m = 0.136$, $R_1 = 22k\Omega$, $R_2 = 90k\Omega$, $C_E = 3\mu F$,
$C_C = 1.2\mu F$

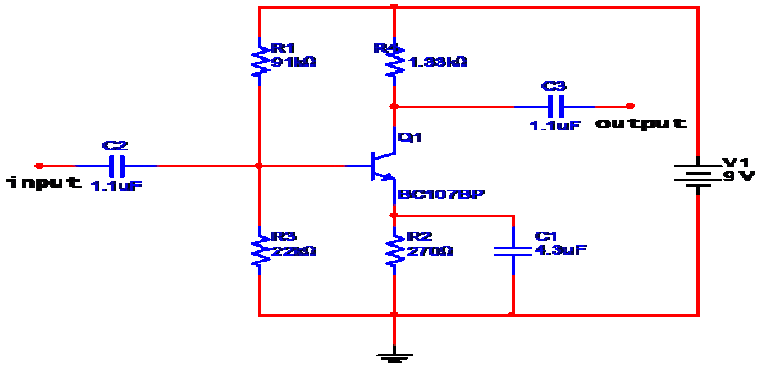

Fig. 4: Single Stage CE

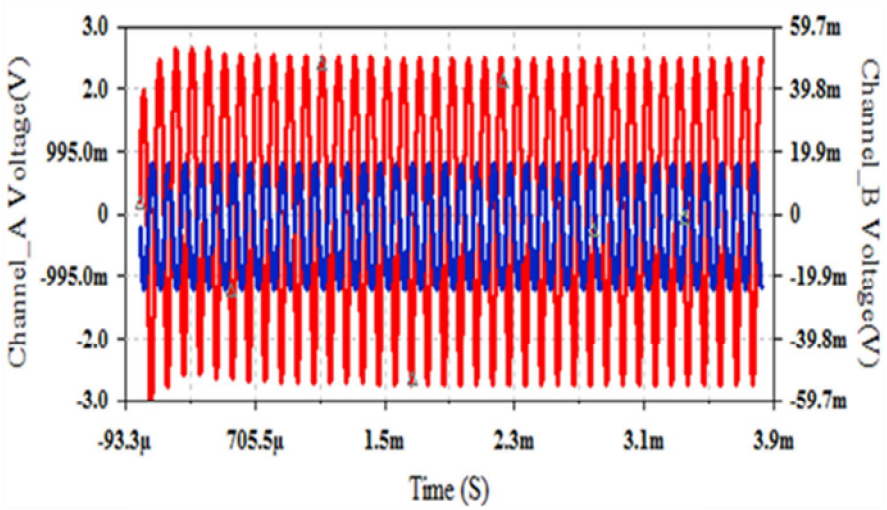

Fig. 5: Simulated Waveform of CE

THE DISTRIBUTED OSCILLATOR

For the transmission line (LC filter) used in designing the distributed oscillator (Fig. 6), the components values used were evaluated using the procedure equations as in (Lee, 2004) and are:

$C_1 = C_7 = 144pF$, $C_3 = C_5 = 574pF$, and $L_2 = L_6 = 992\mu H$, $L_4 \approx 16\mu H$

In forward-gain mode, the forward path can have an overall gain larger than unity while the gain of each transistor may be less than one. To sustain oscillations, the output of the collector line is fed back to the input of the base line. When collector supply voltage V_{CC} is switched on, the capacitor C_1 and C_2 are charged. These capacitors C_1 and C_2 discharged through L setting up Oscillations frequency:

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{LC_1} + \frac{1}{LC_2}} \qquad (21)$$

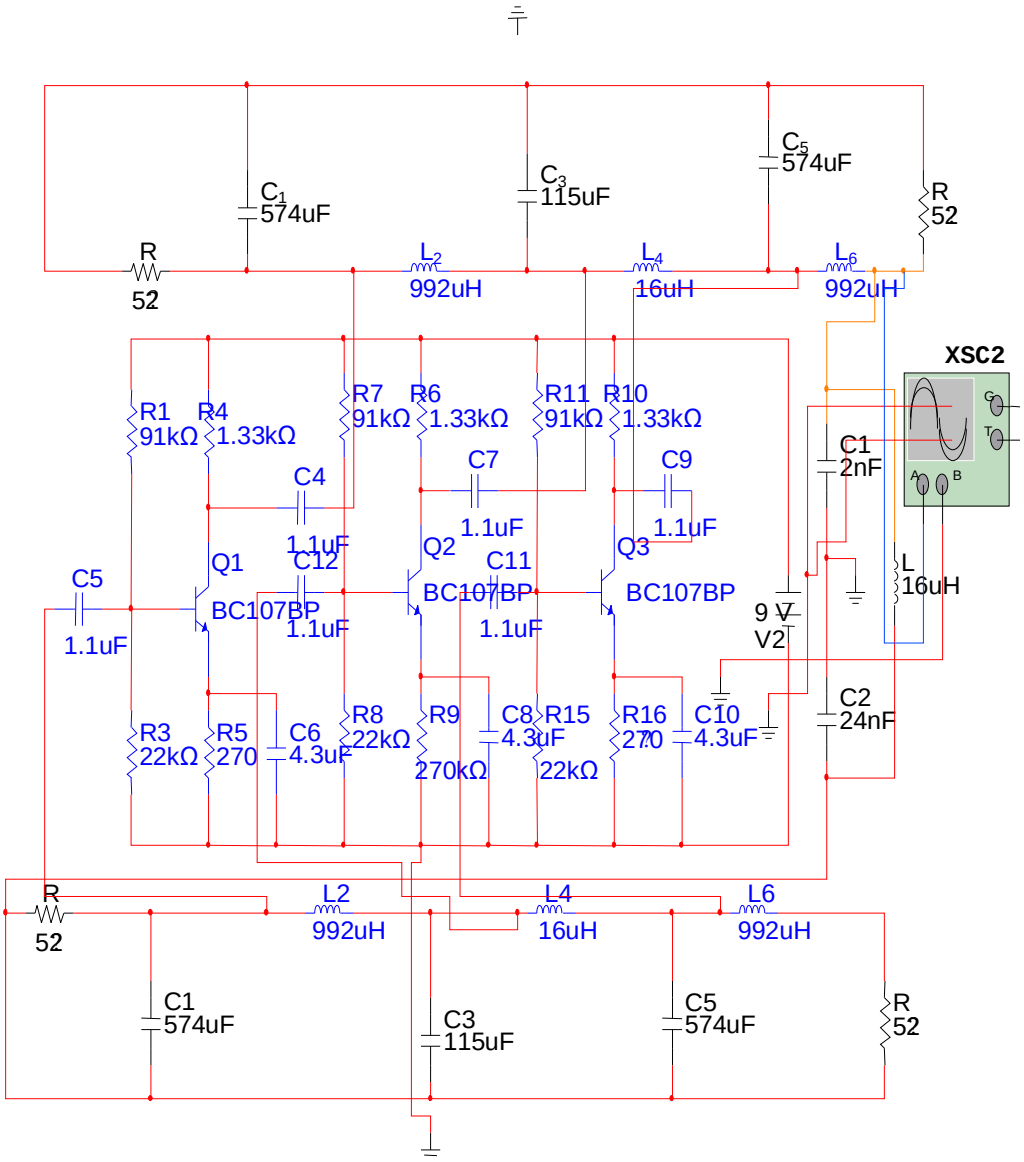

Fig. 6: The distributed oscillator

The amplified output in the output transmission line is of the same frequency as that of the oscillator circuit (LC tank). This amplified output in the collector is supplied energy from the circuit to make up for the losses occurring in it. If $A\beta$ exceeds unity, oscillations are sustained in the circuit. The simulated waveform for the distributed oscillator is shown in Fig. 7.

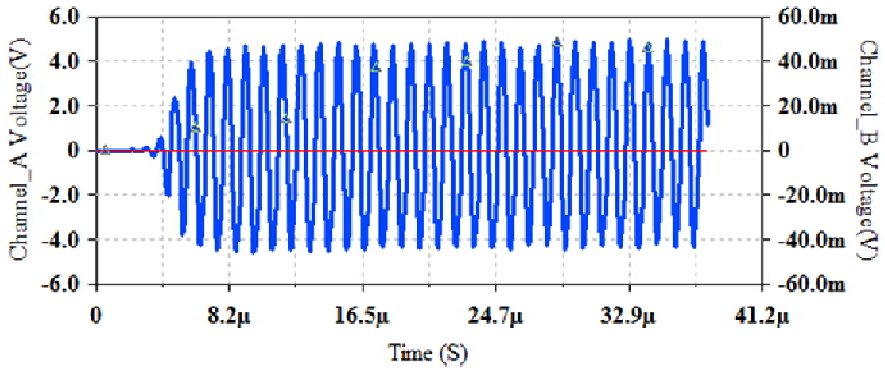

Fig. 7: Simulated waveform for the distributed

FREQUENCY RESPONSE OF CE AMPLIFIER

Having obtained all the component parameters of the amplifier, its frequency response was obtained by plotting a graph of gain $\frac{V_2}{V_1}$ in (dB) versus frequency (Hz) and the bandwidth of the amplifier calculated using the expression

$$Bandwidth\ (BW) = f_H - f_L \quad (22)$$

where f_H and f_L is the higher and lower cut-off frequencies respectively, for n identical stage. The bandwidth is obtain as (Molvino, 1984)

$$B_n = B\sqrt{2^{\frac{1}{n}} - 1} \quad (23)$$

where B_n is overall bandwidth and B, bandwidth of one stage. Normalized filters can be converted into filters which meet arbitrary cut-off frequency and impedance level specifications.

Frequency response of single stage, two stages, three stages amplifier and distributed oscillator were obtained from the simulated data and the graph of gain (dB) verses frequency (Hz) plotted (Figures 8 – 11), from which the bandwidth was in each case obtained.

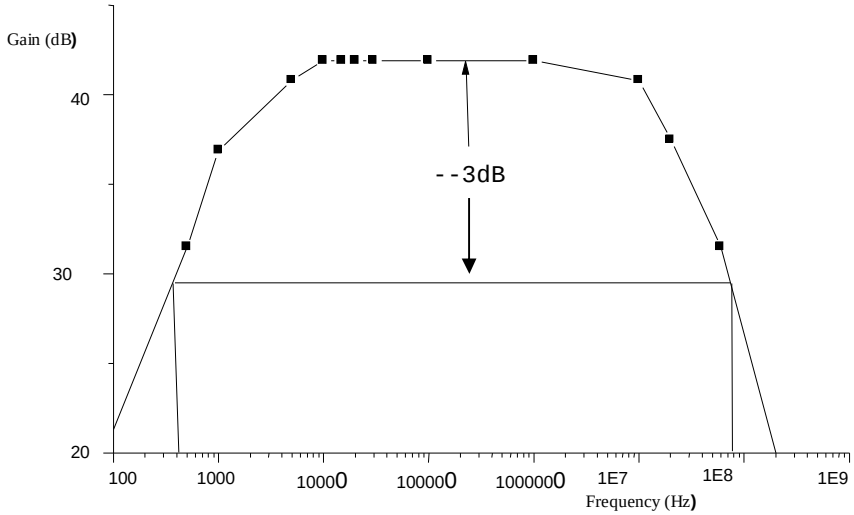

Fig. 8 :Frequency response curve for single stage CE amplifier

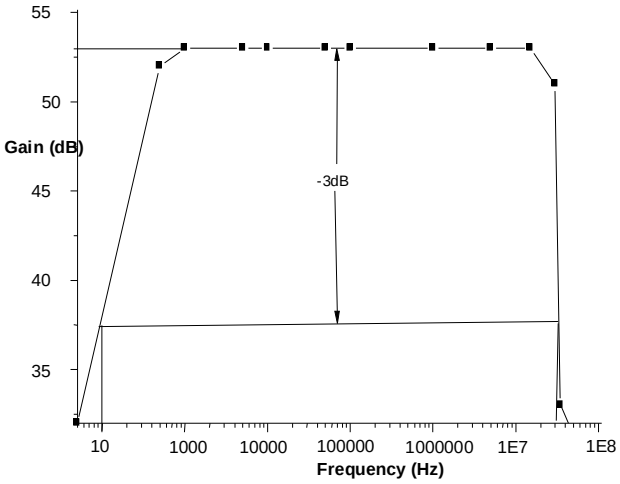

Fig. 9:Frequency response curve for two stages CE amplifier

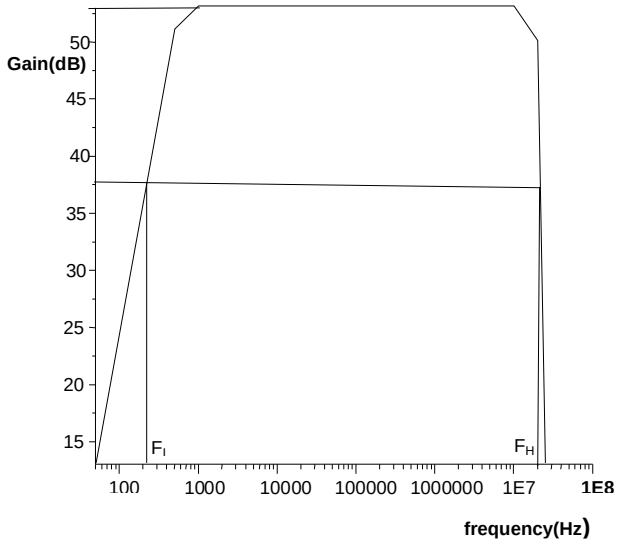

Fig. 10: Frequency response curve for three stages CE amplifier

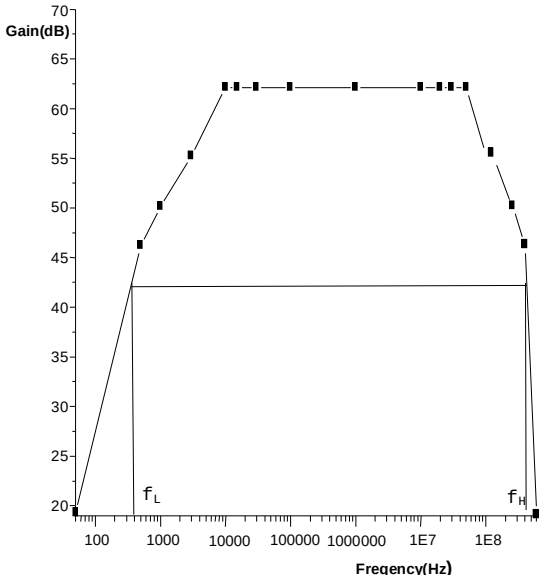

Fig. 11: Frequency response curve for distributed

Table 1: Measured parameters from frequency response curves for each type of amplifier

Amplifier	Mid-gain (dB)	F_L (Hz)	F_H (Hz)	Bandwidth (Hz)	Gain Bandwidth Product (MHz)
Single Stage	50.64	1037.57	37045150.9	37044113.33	1875.14
Two Stages	52.9	97.15	34236819	34236721.85	1811.12
Three Stages	53	212.56	19926946	19926733.44	1056.12
Distributed	62.04	404.84	409107070	4091066652	25380.78

DISCUSSION AND CONCLUSION

From the result obtained in table 1 above, it can be seen that the bandwidth decreases as the number of stages increases for the conventional way of circuits design. That is, the bandwidth of single stage (37044113.33Hz) is greater than that of two stages (34236721.85Hz) and three stages (19926733.44Hz) respectively. The bandwidth of the distributed amplifier (4091066652 Hz) is even far greater than that of the single stage. This really justified the problem of gain-bandwidth trade off and also justified that distributed circuit methodology can alleviate the problem. The distributed amplifier was simulated at frequency of 10 kHz which gives good signal purity as depicted in figure 7, this amplifier introduces delay as the signal propagate through the length of the transmission lines. The distributed oscillator makes use of the delay to enhance sustainability as well as the stability of oscillation. It was also observed that there is trade between bandwidth and the delay. The waveform of the oscillator, which is also good, shows amplitude of approximately 6V. The simulated results show that the oscillator operates at 26MHz, dissipating 15mW power and has good signal purity, therefore meeting design goals.

\In conclusion, a silicon bipolar distributed oscillator operating at high frequency was designed. Special attention was paid to transmission line using Butterworth LC filter that largely play role in the performance of distributed oscillators The idea of a distributed amplification methodology towards design of bipolar distributed oscillator is found viable in high frequency region. Distributed oscillators are used in many RF and high data rate communication systems including Cellular phones, pulsed radar systems, optical receivers and so A BC107 transistor was used in this research work; if a transistor of wider band can be used it will increase the gain and bandwidth and which in turn increases the stability of the oscillator The single inductor found in the phase shift circuit can be replaced by a series L-C combination; this can improve the frequency stability and eliminates the effect of transistor parameters on the operation of the circuit.

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