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Full Length Research Article

# MODELLING BACKSCATTERING EFFECTS IN NANOSCALE CMOS TRANSISTORS USING DRIFT DIFFUSION SIMULATIONS WITH MASTER 4

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**ABSTRACT**
The effects of strain engineering and gate length optimization on the electrical performance of MOSFETs have been examined using Advanced Master 4 simulation software. A tensile strain of 1.5% was applied along both the "x" and "y" directions, with fixed boundary conditions at the source and drain, allowing for strain variation across the channel. All simulations were conducted at room temperature (300 K), to evaluate the influence of strain and channel length variation on electron mobility and overall device behavior. The results revealed a significant improvement in electron mobility for strained devices, increasing from 3.40 X 10-24cm²/Vs in unstrained devices to 4.18 X 10-24 cm²/Vs in strained ones. Additionally, shortening the channel length from 25 nm to 10 nm enhanced both injection velocity and drive current, with strained devices achieving a higher injection velocity of 6.80 X 104 m/s compared to 6.30 X 104 m/s in unstrained devices. The I-V characteristics, on the other hand indicated a substantial increase in on-current for strained MOSFETs, demonstrating enhanced performance due to improved ballistic transport and reduced backscattering effects. Further analysis of the F-carrier distribution function showed sharper peaks in strained devices, signifying higher carrier concentrations and minimized scattering which is a crucial factor for achieving quasi-ballistic transport. Moreover, the simulations highlighted the impact of strain and gate length scaling on the conduction band structure, with strained devices consistently showing superior performance.

**Keywords:** *Backscattering, MOSFET, carrier transport, quasi-ballistic and transistor*.

## INTRODUCTION

Silicon metal-oxide-semiconductor field-effect transistors (SiMOSFET) have been the fundamental building block of integrated circuits for the past several decades. However, as conventional MOSFETs scale to channel lengths below 10 nm, carrier transport in the inversion layer can no longer be adequately modeled using classical drift-diffusion equations (Lundstrom, 1997). At these nanometer scales, quantum mechanical effects like tunneling, carrier quantization, and backscattering become critical to accurately predict device behavior and performance (Fischetti *et al.,* 2001). Backscattering refers to the scattering of carriers into reverse directions due to interactions with photons, ionized impurities, interface roughness, and other carriers. This significantly degrades drive current in nanoscale MOSFETs, presenting challenges for continued scaling (Neophytou *et al*., 2008).

Initial simulations of nanoscale transistors using ballistic quantum transport models provided optimistic performance projections by ignoring carrier scattering (Chaudhry A., 2010). However, experiments showed significant degradation versus ballistic predictions in fabricated nanowire (Neophytou *et a*l., 2008), ultra-thin body, and FinFET (Auth *et al*., 2012) devices due to backscattering. This highlighted the need to incorporate scattering into quantum transport simulations (Lundstrom, 2000). Recent works calculated backscattering rates using Fermi's golden rule, considering the carrier energy and scattering angle for interactions with phonons, impurities, interface roughness and other carriers (Kim *et al*., 2015; Mamaluy *et al.,* 2016; Jin *et al.,* 2009). The scattering rates are included in the carrier mobility and continuity equations, which are solved along with Poisson's equation self-consistently to capture interdependence between transport and electrostatics (Saint-Martin *et al*., 2006).

As transistors continue to shrink in size, traditional models like drift-diffusion equations no longer capture the full picture of how carriers move through a channel. One of the main challenges at the nanoscale is backscattering where carriers are scattered back toward the source due to interactions with phonons and impurities. This effect significantly reduces the drive current in devices like MOSFETs (Eshraghian et al., 2001; Jin et al., 2009).

Early attempts to model this behavior used ballistic transport equations, which provided some insights but fell short under real-world conditions. More advanced models, such as those based on the Boltzmann transport equation and Poisson–Schrödinger solvers, have since been developed. These tools have helped researchers understand the impact of backscattering on performance metrics like drive current and transconductance (Kedzierski et al., 2008; Neophytou et al., 2008; Kim et al., 2015). Strategies like strain engineering and the use of high-mobility materials (e.g., SiGe, GaAs) are now being used to minimize these effects (Mamaluq et al., 2016; Paul et al., 2005; Shin et al., 2010).

The MOSFET remains a cornerstone of modern electronics, with the NMOS variant particularly favored for its simplicity and efficiency. Built on a p-type substrate with n+ source and drain regions, it operates by forming a channel when voltage is applied to the gate. The resulting current flows through defined operational regions—cut-off, triode, and saturation—each governed by gate voltage. As devices become more compact, backscattering doesn't just affect performance; it becomes a key factor in determining how well a device can function under extreme conditions.

Interestingly, backscattering is not unique to electronics. It shows up in other fields too—from radar wave propagation to quantum effects like Anderson localization (Weitzkamp, 2005; Anderson, 1958). This crossover makes it even more important to understand and manage in semiconductor design.

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In recent years, we've made great strides in modeling these effects and improving device performance. Still, challenges remain—especially in balancing speed, power, and accuracy in simulations. This study aims to build on existing research by [insert your specific study goal], helping to refine our understanding and develop better strategies for next-generation semiconductor devices.

## MATERIALS AND METHODS

### Model Design

### Strain Quasi-Ballistic Transport in the Presence of Strain

From the probability ($N_{bal.}$ (x)), we can deduce the probability ($N_{scat}$(x) for an electron to have its first scattering event at position (x):

$$N_{SAT}(x + dx) \ = N_{bal.} - N_{bal.}(x - dx) \qquad (1)$$

Next, we determine the backscattering probabilities ($P_{RC}$(x)) for a ballistic carrier of the

I-th valley, having a scattering event at (x) and being sent back to the source

$$P_{RC}(x) = \frac{T_S\,(x)}{T_S(x) + T_D(x)} \qquad (2)$$

These probabilities are integrated over the entire channel to obtain the fraction of backscattering.

$$F_{RC}{}^{i}\,(x) = \int_0^x P_{RC}\,(x)\,N^{i}{}_{scat}\,(x)dx \qquad (3)$$

The coefficient is deduced by taking into account the carrier distribution:

$$F_{RC}\,(x) = \ P_x\,F^x{}_{RC}\,(x) + \ P_y F_{RC}^y\,(x) + \ P_z F_{RC}^z \qquad (4)$$

And

$$R_C = \ F_{RC}\,(L_{ch}) \qquad (5)$$

Furthermore, the Landauer flux method divides the current into direct fluxes traveling in the positive and negative directions. This method is described and illustrated in Figure 1 below, depicting the directed flux in the process of strained SiMOSFET.

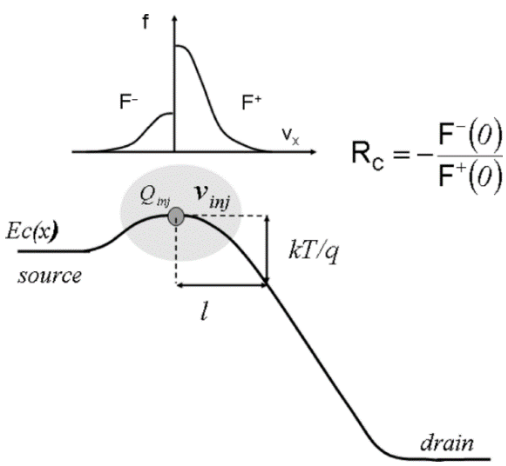


**Figure 1:** Simple one-flux representation of channel transportation in nanoscale MOSFET Unstrain (bulk-Si).

The positively directed flux ($f^+(0)$) is due to thermal diffusion over the channel barrier, whose height is controlled by the MOSFET. The negative directed flux ($f^-0$) arises from the backscattering of the positive directed flux ($f^+(0)$ along the channel. This phenomenon is characterized by a coefficient ($R_C$), which is a real number between 0 and 1, reflecting the degree of transport ballasticity.

Under non-degenerate conditions, the injection velocity can be expressed as:

$$\boldsymbol{V_{thermal}} = \boldsymbol{V_{thermal}}\ \frac{\boldsymbol{1 - R_C}}{\boldsymbol{1 + R_C}} \qquad (6)$$

Here, ($V_{\text{thermal}}$) is the thermal velocity, and ($R_C$) is the backscattering coefficient, determined from the mean-free path and the critical distance over which the channel potential drops by (kT/q:

$$R_C = \frac{l}{l + \lambda} \qquad (7)$$

strain Current Equation

By multiplying the injection velocity by the charge determined from the oxide capacitance $C_{OX}$ and the threshold voltage ($V_T$) (considering short-channel effects), we derive the drain current ($I_d$) equation by taking into account the drain injection at low bias to obtain (7).

$$I_{ds} = C_{ox}\ W(V_g - V_{th})V_{thermal}\frac{1-R_C}{1+R_C}\left[\frac{1-e^{\frac{-qv_{ds}}{KT}}}{1+\frac{1-R_C}{1+R_C}e^{\frac{-qv_{ds}}{KT}}}\right] \qquad (8)$$

where ($V_{ds}$ >> kT), since quasi-ballistic model is the main focus in this research therefore, (9) becomes

$$I_{ds}\,(V_{ds} \gg KT) = C_{ox}\ W\big(V_g - V_{th}\big)V_{thermal}\frac{1-R_C}{1+R_C} \qquad (9)$$

In the ballistic case, where ($R_C$=0), the current is limited by the injection velocity, which equals the thermal velocity. In the simulation, the first step to determine ($R_C$) involves evaluating the potential profile at $V_{ds}$ and $V_{gs}$. This is achieved by assessing the saturation drain voltage and the length of the pinch-off zone while considering access resistance.

Future work should focus on developing an accurate injection charge model for full implementation in a compact model.

From the computed current $I_{ds}$ , we evaluate the potential drop in the access resistance and deduce the potential profile. Using the backscattering model, we determine the injection velocity and subsequently the current $I_{ds}$. This current value is then used to assess the new potential drop in the access resistances, allowing for the calculation of the new injection velocity. This sequence is repeated until convergence of $I_{ds}$ is achieved.

As shown in Figure 2, the schematic structure of the MOSFET channel consists of an n-type substrate with heavily doped $p^+$ regions forming the source (S) and drain (D), while the gate (G) and body (B) complete the device configuration. This geometry enables accurate modeling of carrier transport and is essential for evaluating the influence of backscattering and velocity reduction under nanoscale constraints.

A tensile strain of 1.5% is applied to the channel, modifying the band structure to enhance carrier mobility and reduce scattering rates.

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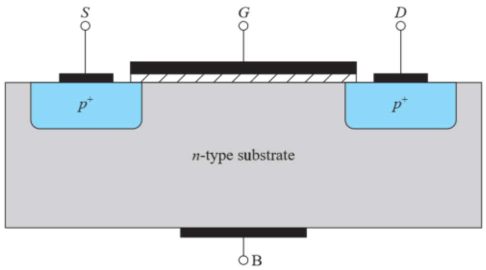


**Figure 2**: Schematic representation of the MOSFET channel

To model the simulation process efficiently, the system begins by initializing the MOSFET parameters such as gate voltage $V_G$, drain voltage $V_D$, and other critical variables, including short-channel effects (SCE) and drain-induced barrier lowering (DIBL). The total inversion charge $Q_{inj}$ is computed based on the gate capacitance and biasing conditions. As shown in Figure 3, the simulation proceeds through iterative loops involving potential calculation, resistance-capacitance (RC) estimation, and injection velocity $V_{inj}$determination. The current $I_{ds}$is computed and evaluated for convergence. If convergence is not met, the loop continues until stable results are achieved, at which point the final drain current is obtained.

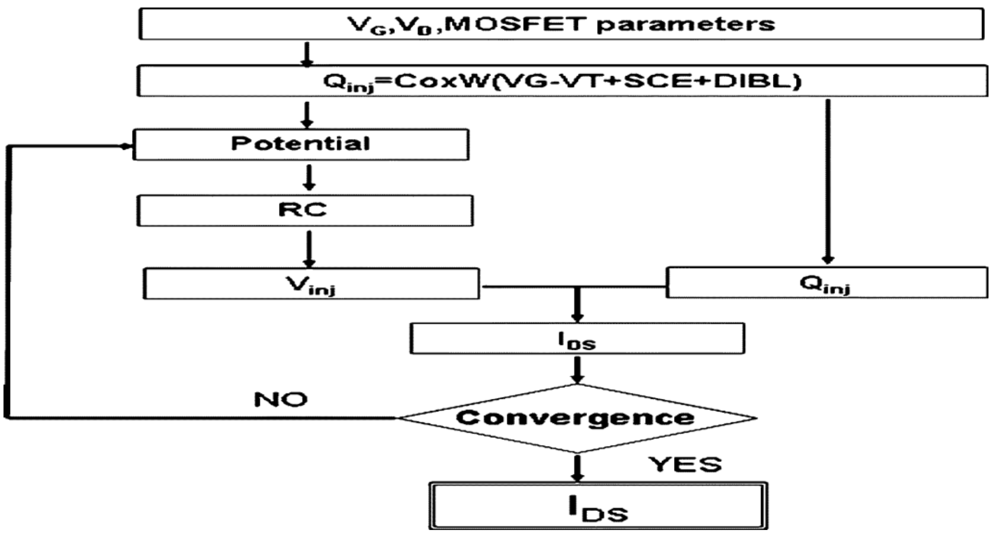


**Figure 3:** Flowchart detailing the simulation workflow, from parameter initialization to result validation.

## RESULTS AND DISCUSSION

### (i). Strain Engineering Effects

Strain engineering has demonstrated a significant positive impact on the performance of semiconductor devices, particularly in two key areas: electron mobility and backscattering probabilities as shown in the table below in Figure 3. The introduction of strain into the devices resulted in a notable increase in electron mobility, with strained devices exhibiting a mobility of 2.81 x $10^{-24}$ cm²/Vs to 2.23 x $10^{-4}$ cm²/Vs observed in unstrained devices. This enhancement can be attributed to several factors. First, strain modifies the band structure, leading to a reduced effective mass of electrons, which facilitates easier movement. Additionally, the application of strain can increase the density of charge carriers, further contributing to improved mobility. Strain also optimizes energy band alignment, reducing barriers for electron transport. These improvements are essential for applications that require high-speed operation and efficiency, highlighting the importance of strain engineering in advancing semiconductor technology.

### (ii). Backscattering Probability

### (a). Strain Engineering Effects

Strain engineering plays a crucial role in reducing backscattering probability, which is vital for enhancing device performance. In strained devices, the injection velocity was measured at 1.03 x $10^4$m/s, significantly higher than the 3.88 x $10^4$m/s observed in unstrained devices. This reduction in backscattering contributes to several important outcomes.

First, by minimizing the likelihood of backscattering, strained devices enable more efficient injection of charge carriers into the active region. This efficiency translates directly into improved overall device performance. Furthermore, lower backscattering enhances the reliability of devices by decreasing the risk of performance degradation.

In addition, the application of strain in nano-scale MOSFETs is a critical strategy to enhance charge carrier mobility and reduce scattering effects, thereby improving device performance.

Table 1 presents a quantitative comparison of transport parameters such as reflection coefficient $\boldsymbol{R_C}$, electron mobility, injection velocity $\boldsymbol{V_{inj}}$, thermal velocity, and mean free path for strained and unstrained devices at a gate length of $\boldsymbol{L_g}$=15 nm. Notably, the strained MOSFET exhibits an increase in injection velocity and mean free path, which are key indicators of enhanced carrier transport due to reduced backscattering.

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**Table 1: Comparison of Transport Parameters for Strained and Unstrained MOSFETs at** $L_g$=15 nm

| Result (at $L_g$ =15nm) | Strained MOSFET (bi) | Unstrained MOSFET (bii) |
|---|---|---|
| Rc (%) | 0.80 | 0.90 |
| Electron mobility(cm$^2$/Vs) | 2.81e$^{-24}$ | 2.23e$^{-24}$ |
| Injection velocity(m/s) | 1.03e$^{+004}$ | 3.88e$^{+004}$ |
| Thermal velocity(m/s) | 1.22e$^{+005}$ | 1.22e$^{+005}$ |
| Mean free path{mfp} | 2.2 | 1.79 |

To complement this numerical analysis, Figure 4 visually depicts the difference in injection velocity profiles between strained and unstrained MOSFETs. The curve for the strained device shows a higher velocity peak, affirming the results in Table 1 and indicating better injection efficiency.

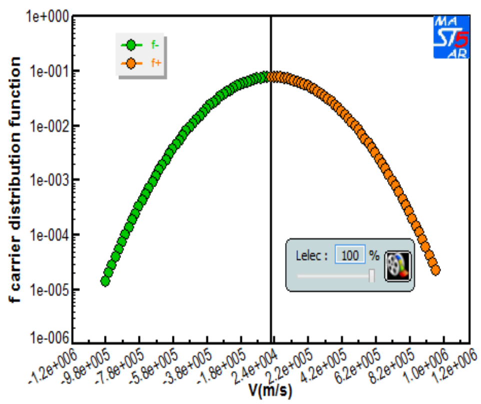



**Figure 4**: Comparison of injection velocity in strained versus unstrained devices at 15nm gate lengths Strain at $L_{ch}$=15nm

Furthermore, the distribution of quasi-ballistic carriers under both conditions is plotted in **Figure 5**. The strained device shows a broader and slightly shifted Fermi-Dirac distribution, suggesting increased energy states conducive to ballistic transport. This shift corroborates the trend in mean free path and further highlights the reduced probability of scattering.

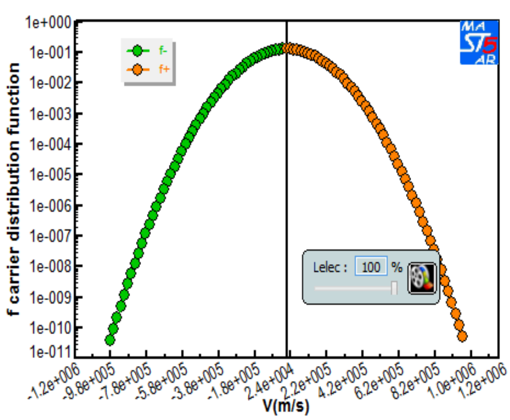



**Figure 5**: Distribution of quasi-ballistic carriers under both conditions

*Unstrain at $L_{ch}$=15nm*Figure 5: strain and unstrained effect of F-Carrier distribution of Quasi ballistic strain at $L_g$ = 15nm and Unstrain at Lg 15nm

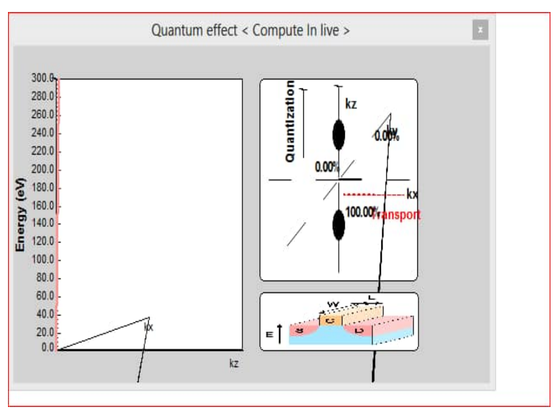
**(b). Quantum Conferment and Gate Length Scaling**

Shorter gate lengths in semiconductor devices significantly enhance quantum confinement effects, leading to improved performance through several key mechanisms. As gate lengths decrease, the spatial confinement of charge carriers results in increased spacing between energy levels. This effect creates discrete energy levels, which enhances the device's responsiveness to electric fields and enables faster switching speeds. Such characteristics are crucial for high-frequency applications where rapid transitions are essential.

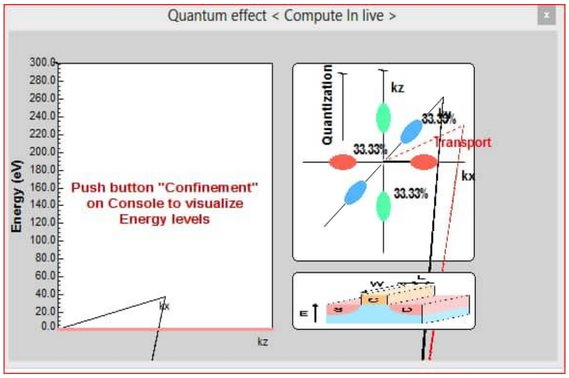
In addition to increased energy level spacing, shorter gate lengths also contribute to improved carrier mobility. This improvement is primarily due to a reduction in scattering events. In smaller structures, electrons encounter fewer obstacles, allowing them to move more freely. Furthermore, the reduced dimensions provide better control over the movement of carriers, minimizing collisions and leading to increased speed and efficiency in device operation. At around 10 nm gate lengths, quasi-ballistic transport becomes a significant mechanism. In this regime, electrons can travel with minimal scattering, resulting in faster transit times and improved current drive. This transport mechanism is vital for next-generation devices, as it enables efficient operation at lower voltages while maintaining high performance.

This behavior is visually illustrated in Figure 6, where subfigure (a) shows the strained device operating at $L_g$=10 nm, and subfigure (b) displays the unstrained counterpart. It is evident that the strained MOSFET demonstrates a stronger quantum confinement effect, with energy levels more widely spaced and more efficient transport characteristics. In contrast, the unstrained device exhibits comparatively reduced confinement and a lower proportion of carriers in the first sub-band, which implies less efficient current conduction.

The difference in the number of electrons occupying confined energy states (as seen in the right panels of each subfigure) reinforces the notion that strain helps promote quantum effects and ballistic transport, which are essential for maintaining performance at such aggressively scaled nodes.




*(a) strain at Lg=10nm*




*(b) Unstrain at Lg=10nm*

**Figure 6:** Simulated Quantum transport for strained and unstrained devices, highlighting the advantages of shorter gate lengths.

**Overall Perfomance Improvements**

Strained devices demonstrated sharper carrier distribution peaks, indicative of higher carrier concentrations and mobility.

i. Mean Free Path (MFP):

MFP increased to 2.2 nm in strained devices compared to 1.79 nm in unstrained ones, reflecting improved transport efficiency.

**Conclusion**

This study emphasizes the critical role of strain engineering and gate length scaling in advancing nanoscale MOSFET technology. Strain significantly reduces backscattering and enhances mobility, while shorter gate lengths support quasi-ballistic transport, optimizing device performance. These findings underline the importance of integrating strain engineering into future MOSFET designs to meet the demands of modern electronic applications.

**REFERENCE**

Auth, C., Allen, C., Blattner, A., Bergstrom, D., Brazier, M., Bost, M., ... & Kolar, P. (2012). A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors. *2012 Symposium on VLSI Technology (VLSIT)*, 131–132. https://doi.org/10.1109/VLSIT.2012.6242455

Fischetti, M. V., Ren, Z., Solomon, P. M., Yang, M., & Lundstrom, M. S. (2001). Six-band k·p calculation of the hole mobility in silicon inversion layers: Dependence on surface orientation, strain, and silicon thickness. *Journal of Applied Physics, 94*(2), 1079–1095. https://doi.org/10.1063/1.1588874

Giusi, G., Iannaccone, G., & Crupi, F. (2011). A backscattering model incorporating the effective carrier temperature in nano MOSFET. *arXiv*. https://arxiv.org/abs/1104.3144

Jin, S., Fischetti, M. V., & Tang, T. W. (2009). Modeling of non-equilibrium transport in nanoscale MOSFETs: Comparison of Monte Carlo and drift-diffusion approaches. *IEEE Transactions on Electron Devices, 56*(11), 2553–2561. https://doi.org/10.1109/TED.2009.2031228

Kim, J., Kim, D., & Shin, M. (2015). Modeling of backscattering in strained-channel MOSFETs using a modified Lundstrom approach. *IEEE Transactions on Electron Devices, 62*(8), 2534–2540. https://doi.org/10.1109/TED.2015.2442151

Kotlyar, R., Kim, R., Stettler, M., Giles, M., & Stasiak, J. (2008). Impact of backscattering on MOSFET design. *IEEE Transactions on Electron Devices, 55*(2), 449–456. https://doi.org/10.1109/TED.2007.913388

Lundstrom, M. S. (2000). Elementary scattering theory of the Si MOSFET. *IEEE Electron Device Letters, 21*(9), 422–424. https://doi.org/10.1109/55.869725

Mamaluy, D., Gao, X., & Tierney, B. (2016). Efficient self-consistent Schrödinger–Poisson solver for quantum transport simulations. *Journal of Computational Electronics, 15*, 1123–1132. https://doi.org/10.1007/s10825-016-0832-3

Mazumdar, K. (2015). Study of the carrier transport in presence of backscattering in InAs nanowire MOSFET. *Applied Surface Science, 336*, 257–262. https://doi.org/10.1016/j.apsusc.2015.01.106

Neophytou, N., Paul, A., & Klimeck, G. (2008). Performance degradation in ultra-narrow Si nanowire transistors due to increased band-to-band tunneling. *IEEE Transactions on Nanotechnology, 7*(6), 710–719. https://doi.org/10.1109/TNANO.2008.2004990

Saint-Martin, J., Bescond, M., & Dollfus, P. (2006). Ballistic transport in double-gate MOSFETs: Influence of electron-phonon scattering. *Journal of Applied Physics, 100*(10), 103712. https://doi.org/10.1063/1.2374686

Vyas, P. B., Van de Put, M. L., & Fischetti, M. V. (2020). Master-equation study of quantum transport in realistic semiconductor devices including electron–phonon and surface-roughness scattering. *Physical Review Applied, 13*(1), 014067. https://doi.org/10.1103/PhysRevApplied.13.014067